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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/747,764	12/29/2003	Rajesh B. Patel	INTEL/17880	9095

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EXAMINER	
ELMORE, REBA I	
ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 06/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/747,764	PATEL ET AL.	
	Examiner	**Art Unit**	
	Reba I. Elmore	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 29 December 2003.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-41 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-41 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 6/26/04.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-41 are presented for examination.

SPECIFICATION

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5, 11-22, 26-35 and 37-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Catherwood.

5. Catherwood teaches the invention (claim 1) as claimed including an address generator as a modulo address generator (e.g., see paragraph 0016 and Figure 1) comprising:

an adder to add a first address component and a second address component to generate an address as adding a current address and an offset (e.g., see Figure 1);

a correction indicator to indicate if the address is correct as calculating the next address to be accessed using the subtractor (element 135) to determine the direction and position for the next address position within the buffer (e.g., see paragraphs 0032-0042); and,

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a control input to modify an operation of the adder as a control input for determining the mode bit (e.g., see paragraph 0025).

As to claim 2, Catherwood teaches the operation of the adder comprises determining a carry bit which updates the current address register thereby affecting the operation of the adder (e.g., see paragraph 0036).

As to claim 3, Catherwood teaches the control input modifies the operation of the adder to force the carry bit to be equal to one of a logic ZERO or a logic ONE (e.g., see paragraph 0028).

As to claim 4, Catherwood teaches the correction indicator generates a control output based on as set of carry bits in the adder with the carry bits being the generation of the adder in conjunction with the subtractor circuitry (e.g., see Figure 1).

As to claim 5, Catherwood teaches the correction indicator generates the control output based on an exclusive OR operation performed on the set of carry bits as the use of logic gates including OR gates, AND gates and exclusive NOR gates (e.g., see paragraphs 0024-0031).

6. Catherwood teaches the invention (claim 11) as claimed including an apparatus comprising:

an instruction scheduler for scheduling a set of address components to process as being inherent since all systems including the system having a hardware based addressing scheme of the reference (e.g., see the background of the invention and the summary of the invention);

an address generator for generating a first address from the set of address components (e.g., see Figure 1); and,

a recovery unit to determine whether the first address is correct or incorrect and if necessary modify an address generator operation by generating a second address from the set of address components as circuitry for determining whether the offset is positive or negative or whether address wrapping is required (e.g., see paragraph 0016).

As to claim 12, Catherwood teaches the address generator has an adder to generate a first and a second address by adding the set of address components (e.g., see Figure 1).

As to claim 13, Catherwood teaches the address generator has a control input to modify an operation of the adder as using the current address and an offset to produce outputs to the subtractor (element 125) and multiplexer (element 155).

As to claim 14, Catherwood teaches the operation determines a carry bit (e.g., see Figures 1-2).

As to claim 15, Catherwood teaches the control input modifies the operation to force the carry bit to be equal to either a logic ZERO or a logic ONE as the use of logic gates including OR gates, AND gates and exclusive NOR gates (e.g., see paragraphs 0024-0031).

As to claim 16, Catherwood teaches the recovery unit sets the control input to a value if the first address is incorrect as the determination as to whether the offset is positive or negative or whether address wrapping is required (e.g., see paragraph 0016).

As to claim 17, Catherwood teaches the value is based on a previous value of the control input (e.g., see Figures 1-2).

As to claim 18, Catherwood teaches the instruction scheduler sets the control input to a value (e.g., see Figures 1-2).

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As to claim 19, Catherwood teaches the address generator has a control output which the recovery unit uses to determine whether the first address is correct as the determination as to whether the offset is positive or negative or whether address wrapping is required (e.g., see paragraph 0016).

As to claim 20, Catherwood teaches the address generator has an adder for generating either the first address and the second address by adding the set of address components with the control output being based on a set of carry bits in the adder (e.g., see Figures 1-2).

As to claim 21, Catherwood teaches the address generator has a first control output and a second control output, the recovery unit determines whether the first address is correct or incorrect based on the first control output and the recovery unit sets the value of the control input based on the second control output (e.g., see Figures 1-2).

As to claim 22, Catherwood teaches the second control output of the address generator is based on a previous value of the control input (e.g., see Figures 1-2).

As to claim 26, Catherwood teaches the instruction scheduler, the address generator and the recovery unit are located in a processor and has a dynamic random access memory coupled to the processor inherently as these are typical and necessary parts of systems having digital signal processors and modulo addressing circuitry/software.

7. Catherwood teaches the invention (claim 27) as claimed including a method of generating an address in a processor as a processor system having a modulo address generator (e.g., see paragraph 0016 and Figure 1), the method comprising:

performing a first addition of a first address component and a second address component to generate a first address as adding a current address and an offset (e.g., see Figure 1);

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determining whether the first address is correct or incorrect as the determination of whether the offset is positive or negative or whether address wrapping is required (e.g., see paragraph 0016); and,

modifying an operation in a second addition of the first address component and the second address component to generate a second address if the first address is incorrect (e.g., see Figures 1-2).

As to claim 28, Catherwood teaches the operation determines a carry bit (e.g., see Figure 1 and paragraphs 0017-0018).

As to claim 29, Catherwood teaches modifying the operation forces the carry bit to a value (e.g., see Figure 1 and paragraphs 0017-0018).

As to claim 30, Catherwood teaches the value is either a logic ZERO or a logic ONE (e.g., see paragraph 0028).

As to claim 31, Catherwood teaches the value is based on a previous value of the carry bit (e.g., see Figures 1-2).

As to claim 32, Catherwood teaches the value is based on either the first address component and the second address component (e.g., see Figures 1-2).

As to claim 33, Catherwood teaches determining whether the first address is correct or incorrect by evaluating a set of carry bits in the first addition of the first address component and the second address component as the determination of whether the offset is positive or negative or whether address wrapping is required (e.g., see Figures 1-2 and paragraph 0016).

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As to claim 34, Catherwood teaches determining whether the first address is correct or incorrect by performing an exclusive OR operation on the set of carry bits as the use of logic gates including OR gates, AND gates and exclusive NOR gates (e.g., see paragraphs 0024-0031).

As to claim 35, Catherwood teaches determining whether the first address is correct or incorrect based on a size of the first address and the second address (e.g., see Figures 1-2).

As to claim 37,Catherwood teaches performing either the first addition and the second addition comprises modifying an operation in either the first addition or the second addition (e.g., see Figures 1-2).

As to claim 38, Catherwood teaches the operation determines a set of carry bits with the modifying of the operation forcing a bit in the set of carry bits to a value (e.g., see Figures 1-2).

As to claim 39, Catherwood teaches the value is either a logic ZERO or a logic ONE (e.g., see paragraph 0028).

8. Claims 1-41 are rejected under 35 U.S.C. 102(b) as being anticipated by Blomgren.

9. Blomgren teaches the invention (claim 1) as claimed including an address generator (e.g., see the abstract of the reference) comprising:

an adder to add a first address component and a second address component to generate an address (e.g., see Figure 1);

a correction indicator to indicate if the address is correct as being able to add adjustment values to the two operand to generate addresses (e.g., see col. 2, lines 48-54); and,

a control input to modify an operation of the adder as the address generator using bypass logic to generate bypass operations when necessary for generating an address (e.g., see col. 4, line 55 to col. 5, line 32).

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As to claim 2, Blomgren teaches the operation of the adder comprises determining a carry bit as the adders being carry-save adders (e.g., see Figures 2 and 6 and col. 3, line 56 to col. 4, line 52).

As to claim 3, Blomgren teaches the control input modifies the operation of the adder to force the carry bit to be equal to one of a logic ZERO or a logic ONE (e.g., see col. 4, lines 4-34).

As to claim 4, Blomgren teaches the correction indicator generates a control output based on as set of carry bits in the adder as the bypass function and logic which utilizes the carry-save adders (e.g., see col. 4, line 54 to col. 5, line 32),

As to claim 5, Blomgren teaches the correction indicator generates the control output based on an exclusive OR operation performed on the set of carry bits as being inherent as the reference teaches using logic gates (e.g., see col. 9, lines 1-12).

As to claim 6, Blomgren teaches the control input is a first control input with a second control input to specify a size of the address as redundant hardware for choosing either 32-bit functionality or 16-bit functionality (e.g., see col. 3, line 55 to col. 4, line 3).

As to claim 7, Blomgren teaches the adder blocks a set of carry bits in the adder based on the second control input as the bypass function (e.g., see col. 4, line 54 to col. 5, line 32).

As to claim 8, Blomgren teaches the correction indicator generates a control output based on the second control input as having the capability of generating and using adjustment values (e.g., see col. 2, lines 48-54).

As to claim 9, Blomgren teaches the adder has a first and second adder wherein the correction indicator generates a control output based on a first set of carry bits in the first adder

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and a second set of carry bits in the second adder (e.g., see Figure 1 and col. 7, line 63 to col. 8, line 19).

As to claim 10, Blomgren teaches the correction indicator generates the control output based on an exclusive OR operation performed on the first set of carry bits and the second set of carry bits as the reference teaching the adders as carry-save adders made of logic gates (e.g., see col. 9, lines 1-12).

10. Blomgren teaches the invention (claim 11) as claimed including an apparatus comprising:

an instruction scheduler for scheduling a set of address components to process as address generation for a sequence of stack instructions (e.g., see col. 7, line 27 to col. 8, line 19);

an address generator for generating a first address from the set of address components (e.g., see Figure 1);

a recovery unit to determine whether the first address is correct or incorrect and if necessary modify an address generator operation by generating a second address if the first address is incorrect as the capability of adjusting or correcting dependent addresses (e.g., see Figures 1-7 and col. 2, lines 48-54).

As to claim 12, Blomgren teaches the address generator has an adder to generate a first and a second address by adding the set of address components (e.g., see Figures 1-7).

As to claim 13, Blomgren teaches the address generator has a control input to modify an operation of the adder as offset and/or displacement values (e.g., see Figures 1-7).

As to claim 14, Blomgren teaches the operation determines a carry bit as being inherent as the adders are taught as carry-save adders (e.g., see the summary of the invention).

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As to claim 15, Blomgren teaches the control input modifies the operation to force the carry bit to be equal to either a logic ZERO or a logic ONE (e.g., see col. 4, lines 4-34).

As to claim 16, Blomgren teaches the recovery unit sets the control input to a value if the first address is incorrect as having the capability of generating and using adjustment values (e.g., see Figures 1-7 and col. 2, lines 48-54).

As to claim 17, Blomgren teaches the value is based on a previous value of the control input (e.g., see Figures 1-7).

As to claim 18, Blomgren teaches the instruction scheduler sets the control input to a value as address generation for a sequence of stack instructions (e.g., see col. 7, line 27 to col. 8, line 19).

As to claim 19, Blomgren teaches the address generator has a control output which the recovery unit uses to determine whether the first address is correct based on the control output as having the capability of generating and using adjustment values (e.g., see Figure 1-7 and col. 2, lines 48-54).

As to claim 20, Blomgren teaches the address generator has an adder for generating either the first address and the second address by adding the set of address components with the control output being based on a set of carry bits in the adder (e.g., see Figures 1-7).

As to claim 21, Blomgren teaches the address generator has a first control output and a second control output (e.g., see Figures 1-7);

the recovery unit determines whether the first address is correct or incorrect based on the first control output as having the capability of generating and using adjustment values (e.g., see Figures 1-7 and col. 2, lines 48-54); and,

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the recovery unit sets the value of the control input based on the second control output as having the capability of generating and using adjustment values (e.g., see Figures 1-7 and col. 2, lines 48-54).

As to claim 22, Blomgren teaches the second control output of the address generator is based on a previous value of the control input (e.g., see Figures 1-7).

As to claim 23, Blomgren teaches the control input is a first control input and the address generator has a second control input for specifying a size of the address as redundant hardware for choosing either 32-bit functionality or 16-bit functionality (e.g., see col. 3, line 55 to col. 4, line 3).

As to claim 24, Blomgren teaches the adder blocks a set of carry bits in the adder based on the second control input (e.g., see Figures 1-7).

As to claim 25, Blomgren teaches the address generator has a control output with the control output being based on the second control input (e.g., see Figures 1-7).

As to claim 26, Blomgren teaches the instruction scheduler, the address generator and the recovery unit are located in a processor and has a dynamic random access memory coupled to the processor as being inherent as the reference teaches both RISC and CISC processing architecture (e.g., see the background of the invention).

11. Blomgren teaches the invention (claim 27) as claimed including a method of generating an address in a processor (e.g., see the abstract of the reference), the method comprising:

performing a first addition of a first address component and a second address component to generate a first address as address components being added to a base address component (e.g., see Figures 1-7);

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determining whether the first address is correct as having the capability of generating and using adjustment values (e.g., see Figures 1-7 and col. 2, lines 48-54); and,

modifying an operation in a second addition of the first address component and the second address component to generate a second address if the first address is incorrect as having the capability of generating and using adjustment values (e.g., see Figures 1-7 and col. 2, lines 48-54).

As to claim 28, Blomgren teaches the operation determines a carry bit as the adders being carry-save adders (e.g., see Figures 2 and 6 and col. 3, line 56 to col. 4, line 52).

As to claim 29, Blomgren teaches modifying the operation forces the carry bit to a value (e.g., see Figures 2 and 6 and col. 3, line 56 to col. 4, line 52).

As to claim 30, Blomgren teaches the value is either a logic ZERO or a logic ONE (e.g., see col. 4, lines 4-34).

As to claim 31, Blomgren teaches the value is based on a previous value of the carry bit (e.g., see Figures 1-7).

As to claim 32, Blomgren teaches the value is based on either the first address component or the second address component (e.g., see Figures 1-7).

As to claim 33, Blomgren teaches determining whether the first address is correct or incorrect by evaluating a set of carry bits in the first addition of the first address component and the second address component as having the capability of generating and using adjustment values (e.g., see Figures 1-7 and col. 2, lines 48-54).

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As to claim 34, Blomgren teaches determining whether the first address is correct or incorrect by performing an exclusive OR operation on the set of carry bits as being inherent as the reference teaches using logic gates (e.g., see col. 9, lines 1-12).

As to claim 35, Blomgren teaches determining whether the first address is correct or incorrect based on a size of the first address and the second address as having the capability of generating and using adjustment values (e.g., see Figures 1-7 and col. 2, lines 48-54).

As to claim 36, Blomgren teaches the size is either a first size or a second size as redundant hardware for choosing either 32-bit functionality or 16-bit functionality (e.g., see col. 3, line 55 to col. 4, line 3).

As to claim 37, Blomgren teaches performing either the first addition and the second addition comprises modifying an operation in either the first addition and the second addition (e.g., see Figures 1-7).

As to claim 38, Blomgren teaches the operation determines a set of carry bits with the modifying of the operation forcing a bit in the set of carry bits to a value (e.g., see Figures 1-7).

As to claim 39, Blomgren teaches the value is either a logic ZERO or a logic ONE (e.g., see col. 4, lines 4-34).

As to claim 40, Blomgren teaches modifying the operation is based on a first address size or a second address size as redundant hardware for choosing either 32-bit functionality or 16-bit functionality (e.g., see col. 3, line 55 to col. 4, line 3).

As to claim 41, teaches the size is either a first size or a second size as redundant hardware for choosing either 32-bit functionality or 16-bit functionality (e.g., see col. 3, line 55 to col. 4, line 3).

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CONCLUSION

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba I. Elmore, whose telephone number is (571) 272-4192. The examiner can normally be reached on Monday and Wednesday from 7:30am to 6:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the art unit supervisor for AU 2189, Reginald G. Bragdon, can be reached for general questions concerning this application at (571) 272-4204. Additionally, the official fax phone number for the art unit is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center central telephone number is (571) 272-2100.

Reba I. Elmore
Primary Patent Examiner
Art Unit 2189

Saturday, June 03, 2006

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